REMARKS/ARGUMENTS

Claims 1-13 are pending. Claim 12 has been amended. No claim has been canceled or added. No new matter has been added.

Claims 8, 9, 11, and 12 were rejected under 35 U.S.C. § 112, first paragraph. Applicants respectfully traverse the rejection. The Examiner indicated that there is no disclosure of configuring "the gate oxide film to prevent diffusion as recited." Applicants assume the Examiner is referring to the "conductive oxide film" recited in claim 8. As described in the Summary, the present inventors researched as to the causes of the current leakage and how that may be minimized. Applicants respectfully note that the specification and figures disclose at numerous locations as to how the current leakage may be reduced. For example, please refer to Figs. 2-9 and corresponding descriptions, where the use of a titanium oxide (gate insulation film) in conjunction with a ruthenium oxide or iridium oxide (gate electrode) reduces the diffusion of conductive elements. The use of a ruthenium oxide or iridium oxide (or conductive oxide) as part of the gate electrode layer is disclosed on page 22, lines 13-17, as a third embodiment (see also Fig. 11). Accordingly, claims 8, 9, 11, and 12 are supported by the specification and figures. Claim 12, nevertheless, has been amended in response to the rejection.

Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hobbs et al. Applicants traverse the rejection. As explained above, the claimed invention relates to reducing or controlling current leakage. The current leakage becomes more and more serious issues as the devices shrink and are forced use thinner and thinner gate oxides.

As technologies advance and devices shrink, the conventional gate oxides that have been suitable in the past for larger devices become unsuitable for smaller devices having thinner gate oxides. That is, silicon oxide that has been most commonly used gate oxide material for many years is believed to be unsuitable for extremely small devices. New improved gate oxide material needs to be discovered, one that would provide better diffusion barrier than the silicon oxide.

Titanium oxide is one of those candidates. However, titanium oxide, as used in conventional device configuration, also could not provide adequate diffusion barrier when

provided as a extremely thin film, e.g., 2-3 nm or less. Therefore, in order to meet the continued demand for smaller devices, a new improved gate oxide material needed to be found or an improved method of using the titanium oxide needed to be found.

The present inventors conducted extensive research to find an improved method of using the titanium oxide. It is generally more cost effective to improve upon conventional composition than developing entirely new gate oxide material. The inventors discovered that when titanium oxide (gate insulation) is used in conjunction with ruthenium oxide or iridium oxide (gate electrode), the diffusion of conductive elements has been significantly reduced (see Figs. 2-9), particularly when the titanium oxide is configured as a rutile structure.

As the Examiner noted that Hobbs disclose a titanium dioxide gate dielectric 62 that is 5-20 nm in thickness, which is considerably thicker than the thickness of 0.9-2 nm being considered in the claimed invention (see claim 5). Not surprisingly, Hobbs is not directed to controlling the diffusion of conductive elements. It is directed to providing a device with a metal gate electrode rather than the conventional polysilicon gate electrode. Hobbs lists numerous possible candidates for gate oxides and even more numerous possible candidates for gate electrodes, without any regard as to their feasibilities.

No where in Hobbs does it provide any motivation or suggestion for using a device that is particularly configured as recited in claim 1. Hobbs does not teach or suggest the use of titanium oxide together with ruthenium or iridium oxide to reduce diffusion coefficient. Accordingly, Hobbs does not teach or suggest "..a gate insulation film formed on one major surface of said semiconductor substrate and including titanium oxide; and a gate electrode film formed in contact with said gate insulation film, said gate electrode film having a dual function of being an electrode and a diffusion barrier, said gate electrode film being configured to minimize diffusion of conductive elements into said gate insulation film to reduce a current leakage via the gate insulation film, said gate electrode film including ruthenium oxide or iridium oxide." The only motivation for such a combination appears to be derived from the present application. Claim 1 is allowable. Claim 2 depends from claim 1 and is allowable at least this reason.

Claims 3-7, 12, and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hobbs in view of Tsunashima. Applicants respectfully traverse the rejection. Tsunashima does not remedy the deficiencies of Hobbs as set forth above. Claim 3 depends from claim 1 and is allowable at least for this reason. In addition, Tsunashima merely discloses the crystallization of titanium oxide. It does not disclose the crystalline structure. As explained in connection with Figs. 2-5, the type of crystal structure affects the diffusion coefficient, e.g., the diffusion coefficient of the rutile structure is less than that of the anatase structure (page 17, lines 7-26). Tsunashima, however, does not appreciate the advantage of the rutile structure in terms of lowering the diffusion coefficient and does not disclose the use of rutile structure, in the manner recited.

Claim 4 recites, "...a gate oxide film formed on one major surface of said semiconductor substrate, said gate oxide film being titanium oxide and having a given crystal structure; and a gate electrode formed over said gate insulation film, said gate electrode including a conductive oxide layer and a metal layer, said conductive oxide layer being provided between said gate oxide film and said metal layer." Hobbs does not disclose a gate electrode comprising a conductive oxide layer and a metal layer, in the manner recited. The Examiner states that Hobbs discloses the recited gate electrode at col. 5, lines 12-30. At that section, Hobbs merely lists a laundry list of possible gate electrode materials and states that a combination thereof may be used. The combination appears to refer to a mixture of material rather than a dual gate electrode structure, in the manner recited. Even if the dual gate is disclosed, Hobbs does not teach providing the conducive metal oxide between the gate oxide film and the metal layer. Tsunashima does not remedy this deficiency of Hobbs. Claim 4 is allowable.

Claim 5 depends from claim 4 and is allowable at least for this reason. In addition, claim 5 recites that the gate oxide film or titanium oxide is about 0.9 nm to about 2 nm. Hobbs does not disclose this thickness range for titanium. As explained in the present application, titanium oxide would not be a suitable gate oxide at such a thickness range due to current leakage. Hobbs does not disclose how to control or prevent the current leakage problem

associated with titanium oxide at such a thickness range. The Examiner noted that Hobbs disclose titanium oxide of 5-20 nm. Tsunashima does not remedy this deficiency. Claim 5 is allowable for this additional reason.

Claim 12 recites, "a gate insulation structure including of a first gate insulation film formed over said semiconductor substrate and including silicon oxide or titanium silicate and a second gate insulation film formed over said first gate insulation film and including titanium oxide; and a gate electrode film formed in contact with said gate insulation structure and including ruthenium oxide or iridium oxide." Neither references disclose a gate insulation structure in the manner recited in combination with ruthenium oxide/iridium oxide.

Claims 8, 9, and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hobbs in view of Gilbert. Applicants respectfully traverse the rejection. Claim 8 recites, "a titanium oxide gate insulation film formed on one major surface of said semiconductor substrate; a gate electrode including conductive oxide film and a metal film, said conductive oxide film being in contact with said gate oxide and configured to serve as a diffusion barrier to prevent diffusion of an element into said titanium oxide to reduce a current leakage via said titanium oxide film; a first capacitor electrode formed on said one major surface of said semiconductor substrate; a capacitor insulation film formed in contact with said first capacitor electrode and exhibiting a high dielectric constant or ferroelectricity; and a second capacitor electrode formed in contact with said capacitor insulation film." Hobbs does not disclose or suggest "a titanium oxide gate insulation film" that is used in conjunction with "a gate electrode" including "a conductive oxide film" and "a metal." Gilbert does not remedy this deficiency. Claim 8 is allowable. Claims 9 and 11 depend from claim 8 and are allowable at least for this reason.

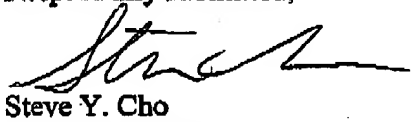
Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Hobbs, Gilbert, and Tsunashima. Applicants respectfully traverse the rejection. Claim 10 depends from claim 8 and is allowable at least for this reason.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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